

# Design and Status of the RF-Digitizer Integrated Circuit

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*An integrated circuit currently under development samples a bandpass-limited signal at a radio frequency (RF) in quadrature and then performs a simple sum-and-dump operation in order to filter and lower the rate of the samples. Downconversion to baseband is carried out by the sampling step itself through the aliasing effect of an appropriately selected "subharmonic" sampling frequency. Two complete RF digitizer circuits with these functions will be implemented with analog and digital elements on one GaAs substrate. An input signal, with a carrier frequency as high as 8 GHz, can be sampled at a rate as high as 600 Msamples/sec for each quadrature component. The initial version of the chip will sign-sample (1-bit) the input RF signal. The chip will contain a synthesizer to generate a sample frequency that is a selectable integer multiple of an input reference frequency. In addition to the usual advantages of compactness and reliability associated with integrated circuits, the single chip will replace several steps required by standard analog downconversion. Furthermore, when a very high initial sample rate is selected, the presampling analog filters can be given very large bandwidths, thereby greatly reducing phase and delay instabilities typically introduced by such filters, as well as phase and delay variations due to Doppler changes.*

## I. Introduction

Conventional digital systems for processing RF signals sample the signal after it has been downconverted from RF to lower frequencies by means of analog mixers and filters. Analog downconversion and its required steps and components can be eliminated by simply sampling the signal at RF, after appropriate bandpass filtering, at a sample rate that is commensurate with the signal carrier. This process, sometimes called subharmonic sampling, aliases the signal directly to baseband.

In addition to the elimination of a number of analog components and the usual advantages of compactness and reliability provided by digital processing, another advantage

can be realized. If the sample rate can be made very large, the phase and delay instabilities due to the analog filters preceding sampling can be made very small by increasing the bandwidths of the filters. For example, with a presampling bandwidth of 600 MHz, the filter delay can be reduced to the order of two nanoseconds in magnitude and a fraction of a nanosecond in instability. In addition, a larger analog bandwidth can greatly reduce phase and delay sensitivity to Doppler variation in the carrier.

This article outlines the design and status of a GaAs integrated circuit (IC) that is designed to sample an RF-bandpass signal at a rate as high as 1200 Msamples/sec (600 Msamples/sec per quadrature component) when the

carrier frequency is as high as 8 GHz. The IC, which will be referred to as the RF digitizer (RFD), will contain a synthesizer that will generate a sample frequency that is a selectable integer multiple of an input reference frequency. This capability has been included in the IC in order to satisfy the stringent stability requirements set by RF sampling. A digital filter consisting of a simple sum-and-dump operation has been included in the IC in order to allow the user the option of reducing an initial high sample rate to a lower value that can be easily processed by subsequent digital circuitry.

Initial use of the RFD chip is planned for the Global Positioning Satellite (GPS) receiver portion of the media calibration subassembly at the Deep Space Network (DSN) antennas. The current chip design contains a pair of RF digitizers with matched synthesizers and samplers. This design greatly improves the differential stability in phase and delay between the two GPS frequency bands (L1 and L2), thereby improving ionospheric calibration.

## II. Subharmonic Sampling

The technique of subharmonic sampling is based on the aliasing that occurs when a signal is sampled at a given rate. If a signal component at frequency  $f_r$  is sampled at the rate  $f_s/n$ , where  $n$  is an integer, that component will be aliased to zero frequency. Signal components with nearby frequencies are aliased to baseband as though they had been downconverted using a mixing signal with frequency  $f_r$ . A more sophisticated downconversion process can be carried out with "half-subharmonic" sampling [1,2,3], in which the sample rate becomes  $f_s = (4f_r)/(2n+1)$ , where  $n$  is a non-negative integer and  $f_r$  is again the frequency component to be downconverted to zero frequency. The advantage of half-subharmonic sampling is that a single sampler at RF, driven by one sample clock, directly produces both quadrature components at baseband with exact quadrature separation. More specifically stated, the sampling process directly produces interleaved cosine (C) and sine (S) samples at baseband in the sequence C, S, -C, -S, C, S, -C, -S, ... The indicated sign reversals on alternate C samples (and S samples) are removed by subsequent IC logic. Because the half-subharmonic approach very simply produces both C and S baseband samples with very exact quadrature separation, this approach has been used on the IC.

## III. Functional Description

A functional block diagram of the RFD is shown in Fig. 1. It is assumed that the input RF signal, which can

have a carrier as high as 8 GHz, is filtered to satisfy the Nyquist criterion as applied to bandpass sampling. That is, if the initial sample rate is  $f_s$  ( $0.5 f_s$  on C and S separately), the sampled signal should have a bandwidth equal to or less than  $0.5 f_s$ . For example, if the initial sample rate is set at the maximum value of 1200 Msamples/sec (Ms/s), then the separate C and S rates will be 600 Ms/s and the maximum input bandwidth can be as high as 600 MHz. The selectable sample rate can range between 4 Ms/s and 1200 Ms/s. Although the initial version of the RFD sign samples (1-bit) the input signal, a second-generation design is planned with 6-bit sampling.

As explained above, half-subharmonic sampling produces interleaved C and S samples with alternating sign reversals. In the IC, the C and S samples are demultiplexed into separate streams and a sign correction is applied to alternate samples of each stream. Each stream is then subjected to a sum-and-dump operation in order to filter the signal and lower the data rate. The sum interval is user selectable, with suggested values of  $N_s = 1, 2, 4, 6, 8, \dots$ , or 30. After summing, the 5-bit sum values can be re-quantized to three levels (-1, 0, and +1), at the user's option. The resulting values and associated clock signal are then output from the IC at a rate of  $(0.5f_s)/N_s$  for each quadrature component.

## IV. Detailed Description

Two RFD's, each incorporating both analog and digital components, will be placed on one GaAs substrate. GaAs was chosen since it is expected to satisfy the stringent speed requirement necessitated by RF sampling. The most critical components of the IC are the frequency synthesizer, an ultra-fast sample-and-hold circuit, and the analog comparator for analog-to-digital (A/D) conversion. The IC will have a complexity equivalent to about 2000 gates, including two matched RFD's, and consume about 10 W. The die will be about 4 mm  $\times$  4 mm in size, and will be packaged in a 149-pin grid array.

The sample-rate "clock," which is generated on-chip by a phase-locked loop synthesizer, is a selectable integer multiple of an input reference frequency between 1 and 200 MHz. The user-selectable multiplier value is equal to  $4N_m$ , where  $4N_m = 4, 8, 12, \dots, 1024$ . Jitter introduced by the synthesizer is expected to be less than 10 psec.

The sampler circuit will consist of two samplers (primary and secondary). The primary sampler, a Schottky diode bridge, satisfies the high-speed requirement and will be constructed with the shortest possible sampling window (about 20 psec). Placed between the primary and

secondary samplers is an amplifier with a gain of 10 dB and a settling time less than 400 psec. This amplifier increases the signal strength to a level (1 V) that is adequate for the secondary sampler and the A/D converter. The purpose of the secondary sampler is to hold the output voltage of the primary sampler at a stable level for an entire clock period ( $1/f_s$ ), thereby allowing the subsequent A/D conversion circuit ample time to settle. The secondary sampler consists of a diode circuit similar to the primary sampler.

The A/D converter translates the signal output by the secondary sampler to a 1-bit signal representing the sign. It consists of a voltage comparator, with a reference voltage of zero and a conversion time of less than 800 psec, operating at a rate of up to 1.2 GHz.

After demultiplexing and sign correction, each sample stream is subjected to a sum-and-dump operation to lower the data rate. To achieve the necessary speed, the sum operation is divided into two successive operations: a two-sample sum (1-bit adder) followed by an  $N$ -sample sum (5-bit adder). Note that this sum-and-dump design leads to total sum intervals that are even integers. The sum interval is user selectable with recommended values of  $N_s = 2, 4, 6, 8, \dots$ , or 30. (Values as high as 510 can be selected, but adder overflow may result.) The user can also elect to bypass the sum and output the initial 1-bit samples at the full initial rate.

The sum values produced by the sum-and-dump operation are effectively 5-bit integers that exit the sum operation in parallel on 5 output pins. (Since the least significant bit, LSB, is always 0, no pin is provided for that bit.) The full, allowable range for the output integers is  $-30$  to  $+30$ , including the phantom LSB.

To allow the user to significantly decrease the bit output rate, the user is given the option of commanding the IC to requantize the sum-and-dump integers from 5 bits to 2 bits, where the two-bit option represents  $-1$ ,  $0$ , and  $+1$ . In this requantization, integer discriminator levels are set so that the sum values of  $-1$ ,  $0$ , and  $+1$  are converted to  $0$ , the values of  $-2$  and lower to  $-1$ , and the values of  $+2$  or greater to  $+1$ . These discriminator levels minimize the

signal-to-noise ratio (SNR) loss caused by the requantization when the sum length is about 20, correlation between initial samples is small, and the single-sample SNR is much less than one.

Data output by the IC can be passed in parallel form or converted to serial form, at the option of the user. The serial output can be made compatible with single-ended emitter-coupled logic.

## V. Status and Plans

Most of the design, simulation, and layout for the IC have been completed and the IC is in the review process. To obtain estimates for IC characteristics (such as parasitic capacitance) that are needed for critical additional simulations of chip design, a test fabrication of a partial chip was submitted during the first quarter of calendar 1991. This partial chip is to be tested during the second quarter of 1991. The fabrication run for the complete 1-bit RFD will be submitted during the third quarter. After low-speed tests have confirmed the basic functionality of the IC, the high-frequency limits will be determined. Detailed measurements of SNR, phase, and delay performance will be carried out using the digital baseband processor of the Rogue GPS receiver [4].

The first implementation of the RFD is planned for the Rogue receiver installed at DSN sites to provide both ionospheric calibrations and precise orbit determination for low Earth satellites. The RFD will provide greater relative stability between signals measured at the two GPS frequencies. The flexible design of the RFD will also allow its use in other applications of high-speed digital processing, such as digital spacecraft transponders and high-accuracy radiometric receivers.

Further improvements are possible for future RFD chip implementations. A laser diode driver would allow the use of a fiber optic cable for transmission of time-tagged digital data. Improving the RF sampling from 1-bit to 6-bit quantization would make the RFD more suitable for low SNR applications such as future very long baseline interferometry receivers and advanced telemetry receivers.

## References

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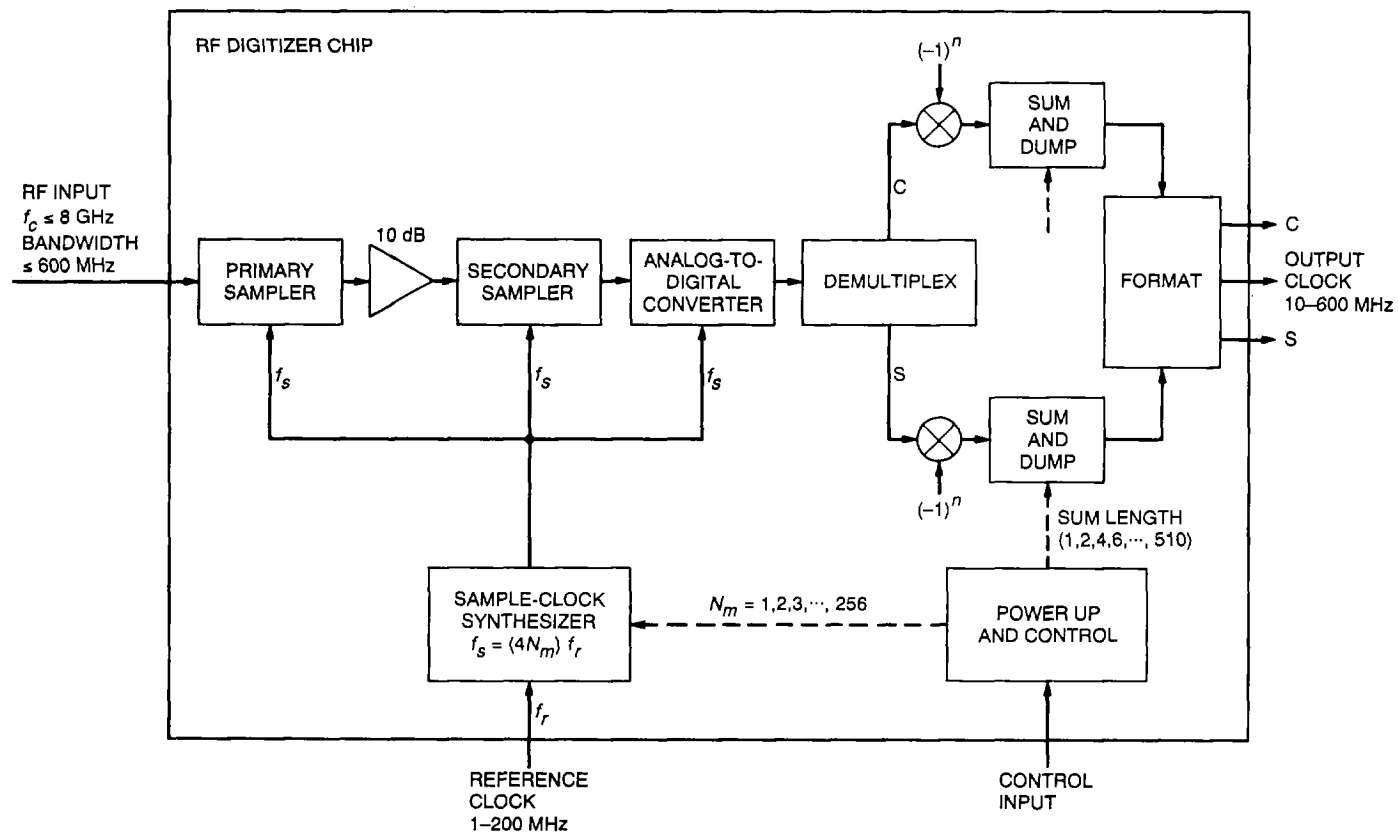


Fig. 1. Functional block diagram of the radio frequency digitizer.